

# IP4286CZ6-TBF; IP4286CZ6-TTY

Integrated 4-channel ESD protection

Rev. 2 — 1 September 2010

Product data sheet

## 1. Product profile

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### 1.1 General description

The devices are designed to protect the capacitive loads of Input/Output (I/O) ports (such as USB 2.0, Ethernet, Digital Visual Interface (DVI), etc.) from being damaged by ElectroStatic Discharge (ESD).

To provide ESD protection to downstream signal and supply components, the devices incorporate four pairs of ultra low capacitance rail-to-rail diodes plus two Zener diodes. This provides protection against contact discharge voltages as high as  $\pm 8$  kV in accordance with IEC 61000-4-2, level 4.

The ESD protection is independent of the supply voltage due to the rail-to-rail diodes being connected to a Zener diode.

The devices are fabricated using monolithic silicon technology and integrate four ultra low capacitance rail-to-rail ESD protection diodes plus two Zener diodes.

### 1.2 Features and benefits

- Pb-free and Restriction of Hazardous Substances (RoHS) compliant
- IEC 61000-4-2, level 4,  $\pm 8$  kV contact discharge compliant ESD protection
- Four input ESD rail-to-rail protection diodes with ultra low input capacitance of 0.6 pF maximum
- Low-voltage clamping due to integrated Zener diodes

### 1.3 Applications

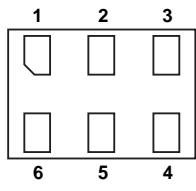
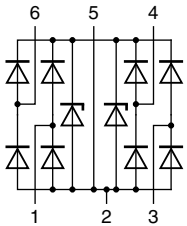
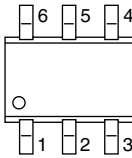
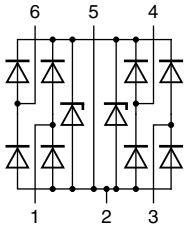
General-purpose downstream ESD protection high-frequency analog signals and high-speed serial data transmission for ports inside:

- PC/Notebook USB 2.0/IEEE 1394 ports
- Cellular phone and Personal Communication System (PCS) mobile handsets
- Digital Visual Interface (DVI)
- High-Definition Multimedia Interfaces (HDMI)
- Cordless telephones
- Wireless data (WAN/LAN) systems
- MID (Mobile Internet Device) and PMP (Portable Media Player)



## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>IP4286CZ6-TBF (SOT886)</b>			
1	ESD protection for I/O signals	 <p>bottom view</p> <p><b>XSON6</b></p>	 <p>018aaa046</p>
2	ground		
3	ESD protection for I/O signals		
4	ESD protection for I/O signals		
5	ground		
6	ESD protection for I/O signals		
<b>IP4286CZ6-TTY (SOT363)</b>			
1	ESD protection for I/O signals	 <p><b>SC-88</b></p>	 <p>018aaa046</p>
2	ground		
3	ESD protection for I/O signals		
4	ESD protection for I/O signals		
5	ground		
6	ESD protection for I/O signals		

## 3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
IP4286CZ6-TBF	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
IP4286CZ6-TTY	SC-88	plastic surface-mounted package; 6 leads	SOT363

## 4. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2, level 4, contact discharge	-	$\pm 8$	kV
$T_{stg}$	storage temperature		-55	+125	$^{\circ}\text{C}$
$V_I$	input voltage		-0.5	+5.5	V

## 5. Characteristics

**Table 4. Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{(I/O-GND)}$	input/output to ground capacitance	$V_I = 3.3\text{ V}$ ; $f = 1\text{ MHz}$	[1][2][3]	0.6	-	pF
$I_{LR}$	reverse leakage current	$V_I = 3.0\text{ V}$	[4]	-	100	nA
$C_{(zd-GND)}$	Zener diode to ground capacitance		[1]	20	-	pF
$V_{BRzd}$	Zener diode breakdown voltage	$I_{test} = 1\text{ mA}$	[1]	6	9	V
$V_F$	forward voltage		-	0.7	-	V

[1] Guaranteed by design.

[2] Route differential pairs to pins 1 and 6, and to pins 3 and 4 for optimal parasitic symmetry.

[3] Pins 1 and 6, and pins 3 and 4 to ground.

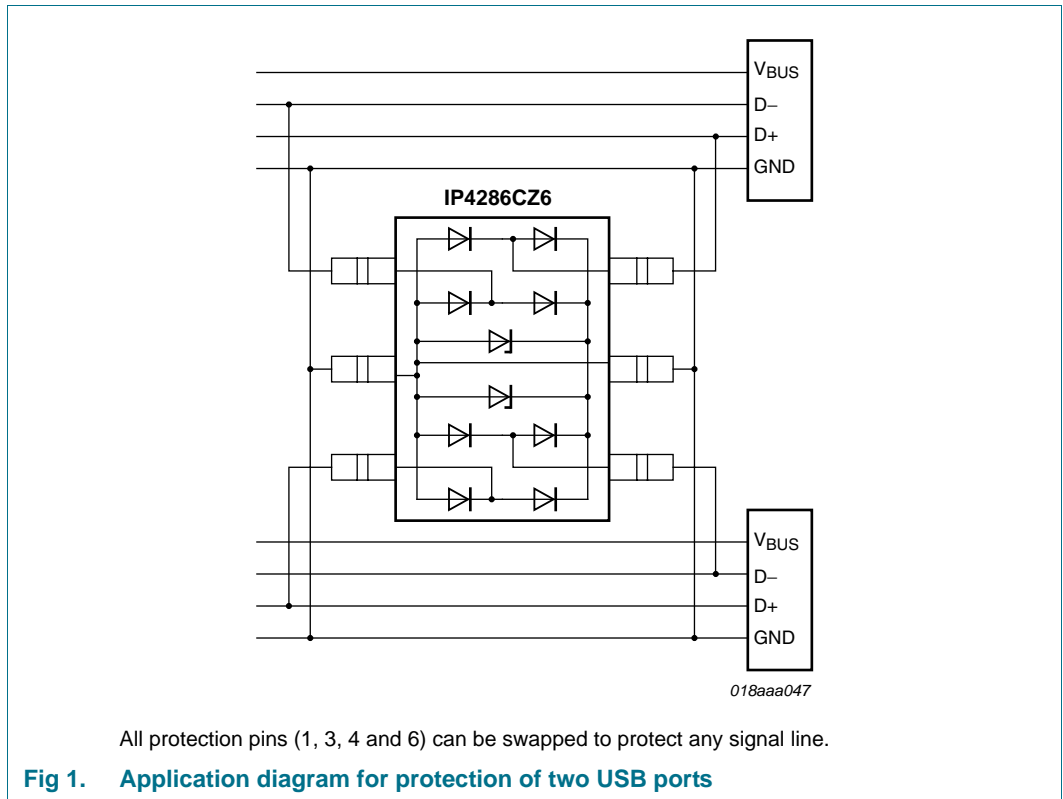
[4] Pins 1, 3, 4 and 6 to ground.

## 6. Application information

### 6.1 Typical application

The devices are capable of protecting both USB data lines of a USB 2.0 port from ESD, and are optimized to protect two USB 2.0 ports simultaneously.

A typical application is shown in [Figure 1](#).



7. Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

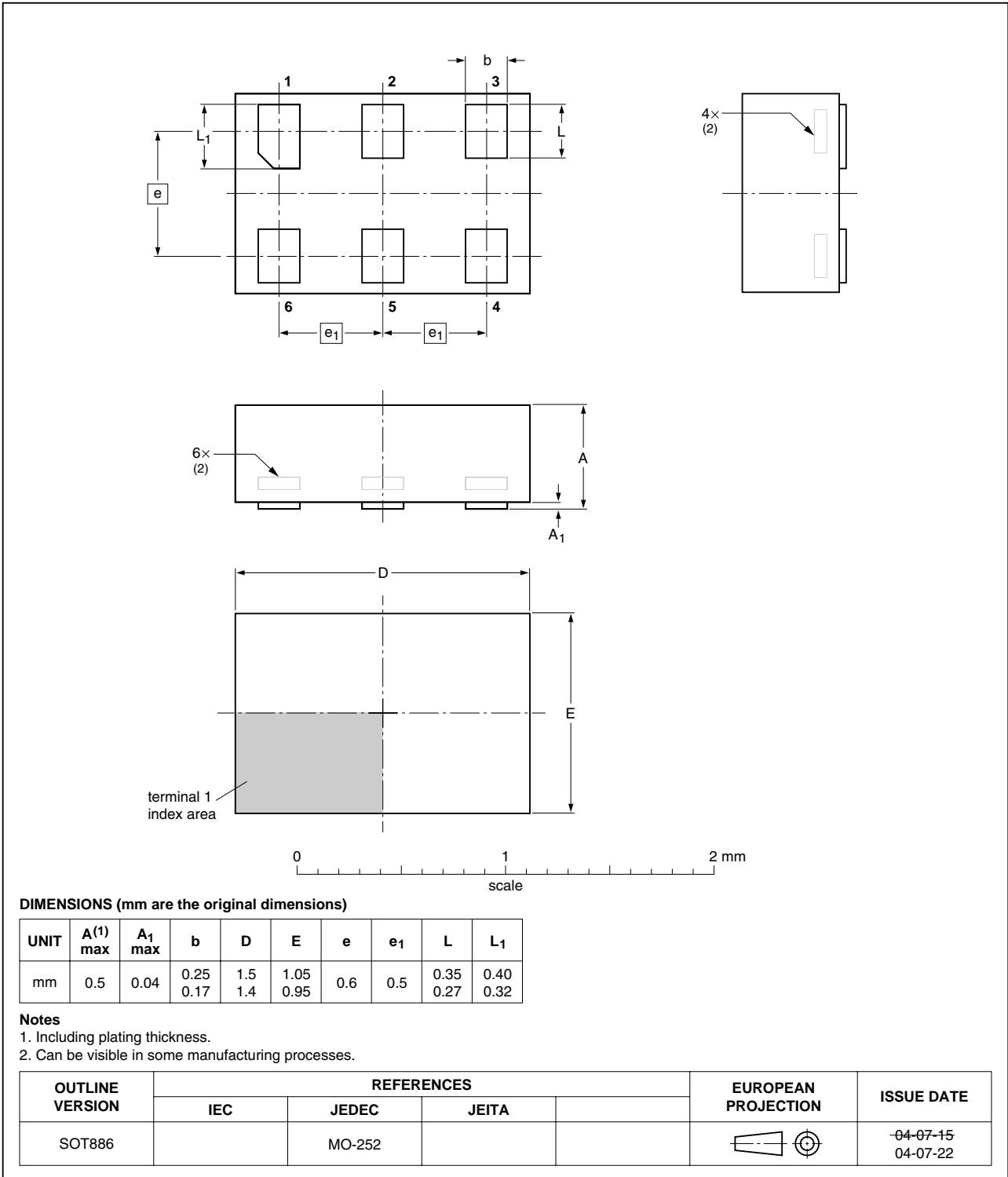


Fig 2. Package outline SOT886 (XSON6/MO-252)

Plastic surface-mounted package; 6 leads

SOT363

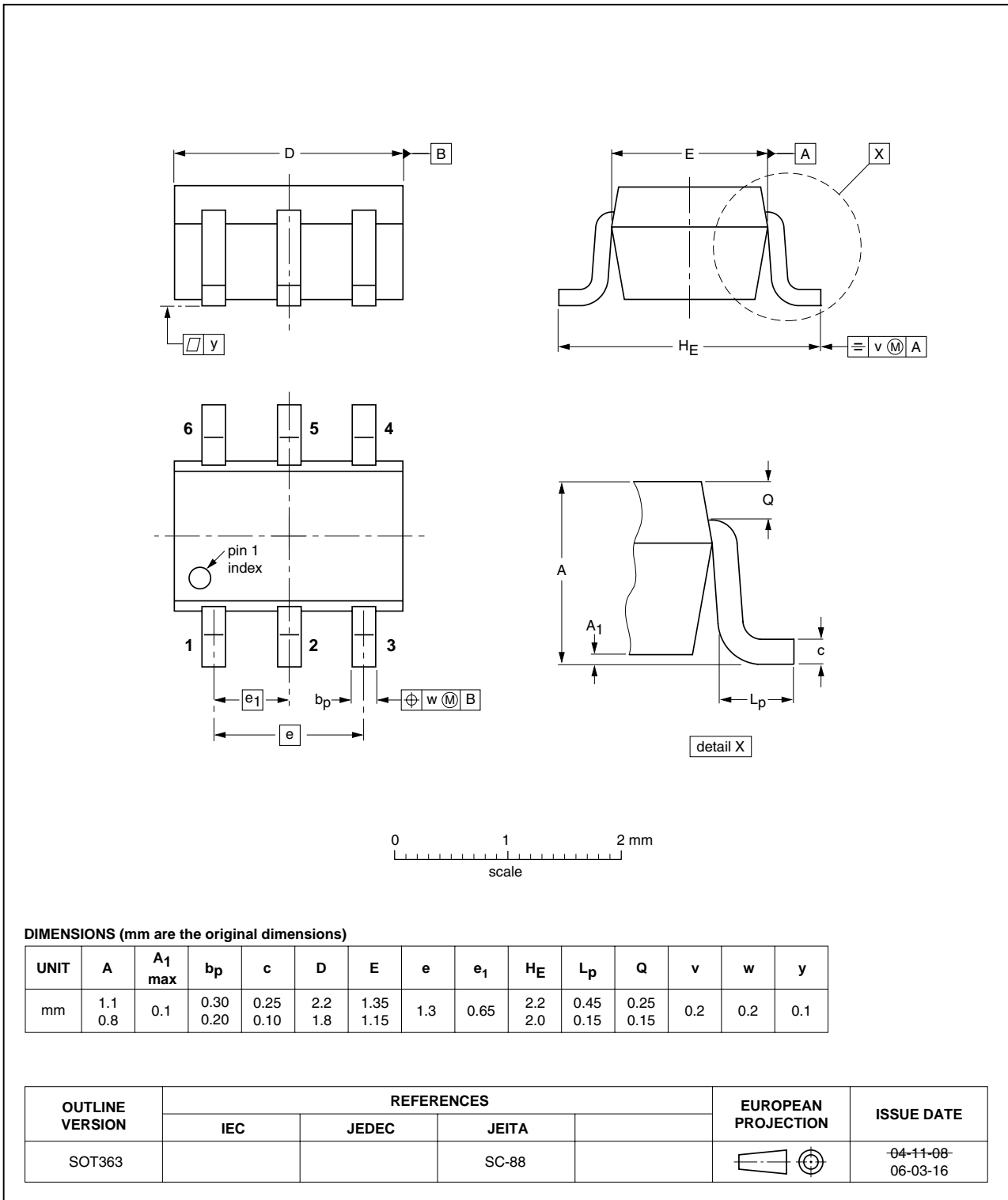


Fig 3. Package outline SOT363 (SC-88)

## 8. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 8.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 8.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 8.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 8.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 4](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 5](#) and [6](#)

**Table 5. SnPb eutectic process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

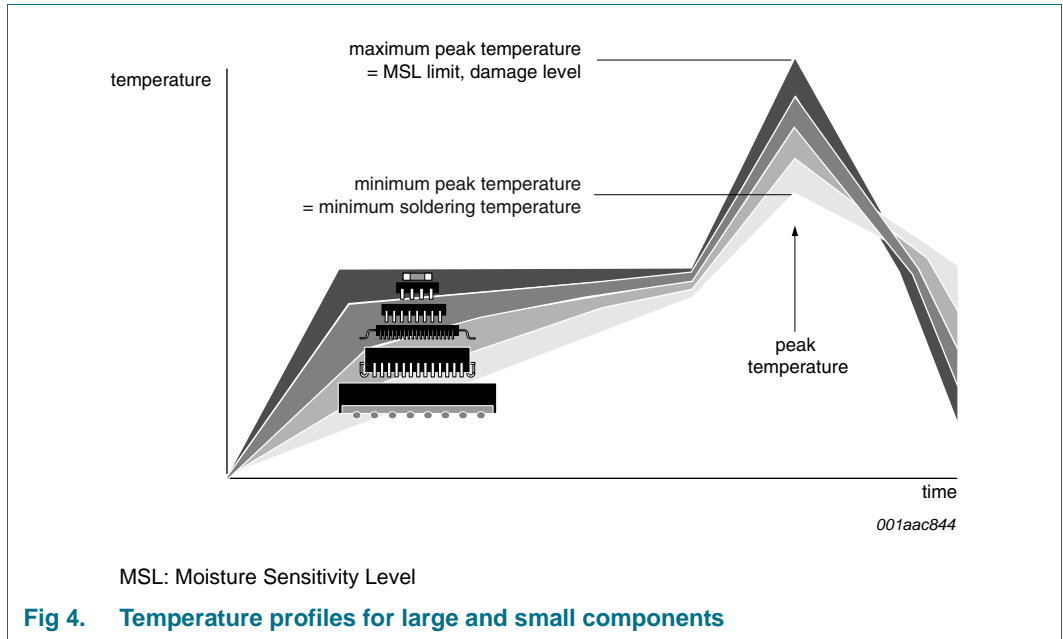
**Table 6. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 4](#).





For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4286CZ6-TBF_TTY v.2	20100901	Product data sheet	-	IP4286CZ6_1
Modifications:	<ul style="list-style-type: none"><li>• Type number IP4286CZ6-TTD deleted.</li><li>• <a href="#">Table 1 "Pinning"</a>: amended.</li><li>• <a href="#">Table 3 "Limiting values"</a>: amended.</li><li>• <a href="#">Table 4 "Characteristics"</a>: amended.</li><li>• <a href="#">Figure 1</a>: updated.</li><li>• <a href="#">Section 10 "Legal information"</a>: updated.</li></ul>			
IP4286CZ6_1	20090420	Objective data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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Date of release: 1 September 2010

Document identifier: IP4286CZ6-TBF\_TTY